# A Highly Capable Arbitrary Waveform Generator for Next Generation Radar Systems

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**Abstract- We are developing an Arbitrary Waveform Generator (AWG) to provide enhanced capability for radar applications. The current design will accommodate two waveform generators on a single unit for dual frequency operation. The basic architecture of this unit employs a Field Programmable Gate Array (FPGA) and a high speed and high precision Digital to Analog Converter (DAC) for direct digital synthesis. This AWG will be capable of up to 450 MHz bandwidth with ability for frequency notching. Phase fidelity of less than 1.2º deviation RMS is also achievable. This AWG operates with lower power consumption as compared with other waveform generators, which is advantageous for future spaceborne applications. This will enable radars to return higher precision data, to be reduced in complexity, and to operate in any band without interfering with dedicated bandwidths.**

## I. INTRODUCTION

With the advance of FPGA and DAC technology, highly capable waveform generators can now be realized based on an architecture centered on an FPGA with a large Random Access Memory (RAM) capacity and a high speed DAC. The RAM in the FPGA provides adequate storage for the pulse widths of most radar applications and the high clock rates achievable in the FPGA and DAC allow for generation of high bandwidth waveforms to enable greater radar resolution.

This design also provides the greatest degree of flexibility in waveform shape as the output waveform is constructed from digital samples that can be programmed directly with 12 bit precision. This precision in the DAC also results in output waveforms that have very high fidelity as shall be demonstrated in the performance characteristic data section.

Systems also often need dual frequency generation capabilities with synchronization between the two channels. The compact design of this AWG has been exploited to incorporate two waveform generation circuits on a single 6U VME card.

These advantages have been implemented in this unit to produce an AWG that is highly flexible and highly capable in bandwidth, waveform precision, power saving, and mass and space saving.

Previous waveform generators used in radar systems have either been units based on numerically controlled oscillators (NCOs) or they have been AWGs that are excessive in mass and power consumption. The NCO-based digital chirp generators (DCG) do not have as much flexibility in generating different waveforms as does AWGs because they operate from a sinewave lookup table. AWGs store digital samples of the entire waveform in RAM which allows for generation of waveforms of arbitrary shape. Table 1 shows a comparison between previous models of waveform generators and the unit being described in this paper. The first DCG has a ITT Microwave (formerly Stanford Telecom) Digital Chirp Synthesis STEL-2375 [1] as the core component. The second DCG uses an Analog Devices Direct Digital Synthesizer, AD9858 [2] to generate chirps. The third waveform generator is the Tektronix manufactured test equipment that was flown on an airborne platform for the GeoSAR project. Even though the Tektronix instrument is an AWG, its size and weight makes it unsuitable for spaceborne radar applications.

| | **NCO-Based DCG (STEL-2375)** | **NCO-Based DCG (AD9858)** | **Tektronix AWG2040 [3]** | **AWG (this work)** |
|---|---|---|---|---|
| Heritage | SIR-C, SRTM | WSOA, Aquarius | GeoSAR | UAV SAR |
| Clock | 1 GHz | 1 GHz | 1 GHz | 1.3 GHz |
| Bandwidth | 400 MHz | 400 MHz | 400 MHz | 450 MHz |
| Pulsewidth | > 1 msec | > 1 msec | 1 msec | Up to 80usec |
| Amp Flatness | 0.5 dB | 0.5 dB | | 0.5 dB |
| Amp Ripple | 0.1 dB | 0.1 dB | | 0.1 dB |
| In-Band Spurs | < - 40 dBc | < -45 dBc | < -45 dBc | < -45 dBc |
| Out-of-band Spurs | < -60 dBc | < -60 dBc | | < -60 dBc |
| DC Power | 24W | 12W, 10W | 300W | 6W * |
| Mass | 750g | 700g | 10.5 kg | 200 g * |
| Radiation | Rad-Hard (GaAs) | Rad-Tolerant (CMOS) | | **TBD** |
| Maturity Level | Very High | High | N/A | Medium |

**Table 1 – Chirp Generator Comparisons for Spaceborne and Airborne Systems**

* NOTE: The mass and power is for a single AWG (see figure 1) not the dual AWG discussed later in this paper.

## II. FUNCTIONAL THEORY

The purpose of the AWG developed here is for chirp and calibration (cal-tone) waveform generation for the radar system. The chirp waveform is usually a linear frequency sweep waveform sometimes with notching to prevent interference with dedicated bands. The cal-tone is a constant frequency sinewave generated for calibration of the radar system.

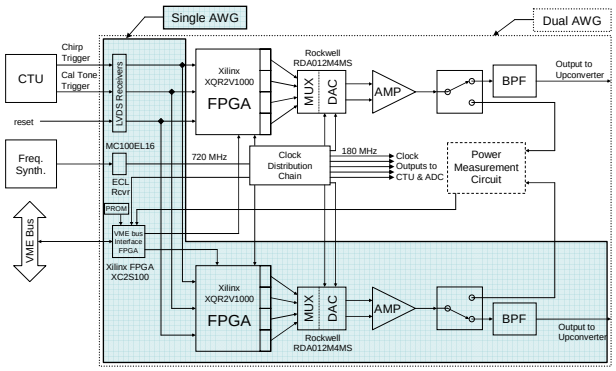


Figure 1 - AWG Block Diagram

Our AWG is a RAM-based waveform generator. This design utilizes the high speed DAC for direct signal generation. Figure 1 shows the block diagram of this AWG. The 12 bit samples of the desired waveform are stored in the RAM within the FPGA. The desired chirp waveform is loaded into the FPGA RAM via the VME bus. The FPGA begins outputting samples to the DAC for the signal waveform when triggered by the chirp trigger. Similarly, the cal-tone parameters can be loaded into the FPGA via the VME bus and the signal waveform is outputted upon the cal-tone trigger. FPGA output is clocked by the slower clock at 180 MHz, 4 samples or 48 bits are outputted at a time to the DAC. The DAC is clocked at 720 MHz and sequentially selects samples with an internal multiplexer (MUX). The generated analog signal is amplified, filtered and then outputted to the upconverter.

Even though the maximum clock frequency of this AWG is 1.3 GHz we use 720 MHz for the system clock because that is the specified clock frequency for our application.

Each radar pulse is synthesized by the AWG and then upconverted to the desired frequency and amplified before transmission. (Note: the upconversion is accomplished external to the AWG.)

The following sections will describe the main output products of the AWG, the chirp and cal-tone waveforms, as well as the frequency limitations of the AWG.

**1. The Chirp Waveform**

The chirp pulse length limit is determined by the amount of FPGA RAM available. The pulse duration is related to the RAM size by the following equation:

$$Pulse\,Duration = \frac{RAM\ size}{720MHz * 12\,bits/sample}$$

For the Xilinx QPro Virtex II XQR2V1000 FPGA used here, the maximum RAM is 720 Kbits, leading to a potential maximum pulse width of about 81 µsec with some RAM set aside for cal-tone waveform storage.

**2. The Cal-Tone Waveform**

Due to the length of typical cal-tone pulses it would be inefficient to store the whole cal-tone signal in the RAM. Since the cal-tone waveform is a constant frequency sinewave it can be generated by repeating a single segment numerous times. The only requirement would be that the start and end phase of the segment need to be consistent in order to maintain continuity in the generated waveform. In order to minimize quantization noise, a large number of unique samples will be used to specify the segment. This is necessary because if too few samples were chosen over the cal-tone segment length the same quantization errors would occur over each repetition of the cal-tone segment.

**3. Frequency Limits**

The AWG output has a theoretical frequency limit, called the Nyquist limit, of 50% of the sampling frequency. However, the actual waveform output will begin to degrade at a lower frequency because real DACs need more samples per period to adequately reconstruct the waveform. During laboratory tests of this AWG it was found that the waveform maintained high fidelity up to 35% of the clock frequency. Above this point the waveform began to show a significant increase in phase deviation from the ideal quadratic fit. The current DAC is capable of clock rates of 1.3 GHz which enables generation of output waveforms of greater than 450 MHz bandwidth. This architecture also allows for a very clear upgrade path for greater bandwidth capability as future technology increases the clock rate capability of the DAC.

## III. DESIGN

The overall architectural design of the dual AWG is described in the block diagram in figure 1. The AWG contains two separate waveform generation units with a single synchronous clock distribution chain. The core of each waveform generation unit consists of an FPGA and a high speed DAC. The AWG control is handled by an FPGA that currently is designed to communicate via the VME bus with a host computer. A divided power distribution scheme is also used to enable power to be shut off to portions of the AWG. The following section will detail the function of each of the main components of the AWG.

**1. VME Interface FPGA**

The AWG is controlled by an external host computer. In order to facilitate the communication between the AWG and the host computer, an FPGA is implemented to handle the communication protocols of the VME bus. This FPGA is configured on power-up by an onboard Programmable Read-Only Memory (PROM). The memory address is mapped from the VME address to the AWG address within this FPGA. This allows the host access to the configuration memory and waveform memory of each of the waveform generators. This FPGA also allows the host access to dedicated registers within the main FPGA which

determine the mode of operation as well as the health status of the waveform generators.

## 2. FPGA Design

We chose the main FPGA (XQR2V1000) primarily for its RAM capacity. This FPGA provides adequate RAM and logic for our application while limiting size and power. The chirp and cal-tone sample data are stored in this memory because this memory can be accessed at high speeds.

The other function of this FPGA is for control of the state of the waveform generator. These states correspond to modes of operation for the waveform generator and can be changed by accessing the dedicated registers for each change action.

When the waveform generator is configured and setup to generate the desired waveform the FPGA responds to a chirp or cal-tone trigger as the signal to start sending waveform data to the DAC.

## 3. Interfaces

This AWG communicates with the host computer via the VME bus as has been described in the previous section on the VME interface FPGA. This AWG also receives the chirp and cal-tone triggers, the reset signal and the clock directly from the units generating these signals. The triggers and the reset signals are received in LVDS format and the clock is received as a single ended sinusoid.

The input clock, 720 MHz for our application, is divided down by 4, 180 MHz in our case, for the FPGA on our board. Some extra 180 MHz output clocks are also generated to provide synchronous, low jitter clock sources to the rest of the radar digital subsystem. The output clocks can be used by analog to digital converters (ADCs) on radar receivers for digitizing of the data.

The current design employs conduction cooling as the thermal interface for transfer of heat. The board is equipped with wedge locks and metal rails that contact with the VME card cage to remove heat by conduction.

## 4. Clock Distribution and Synchronization

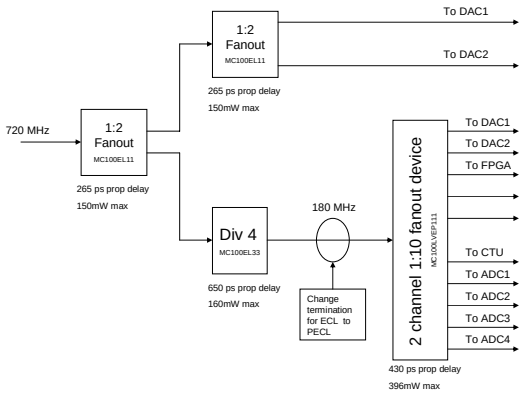


**Figure 2 - Clock Distribution Chain**

An important capability of this AWG is dual waveform generation. This added capability brings the challenge of synchronization of the two waveform generators. This issue is addressed in the design of the clock distribution chain. Figure 2 describes the concept of the clock distribution scheme.

The clock distribution chain supplies the clock to guarantee synchronization of both waveform generators which are derived from the same clock source. The output clocks for the rest of the system are also provided via this specially designed clock distribution chain to achieve low skew between parts and low jitter on the clocks throughout the system.

## 5. Power Distribution

The AWG is designed with capability for partial power shutdown in order to save power when only one waveform generator is active. The AWG is broken up into three main power sectors. The first are the power planes that are always powered when power is supplied to the board. The other two are the power planes being supplied to waveform generator 1 and 2. Figure 3 shows the division of power sectors on the AWG board with the main components powered within each power sector as well as the power levels of the power planes within each power sector. The VME interface FPGA controls the powering of power sectors 2 and 3.

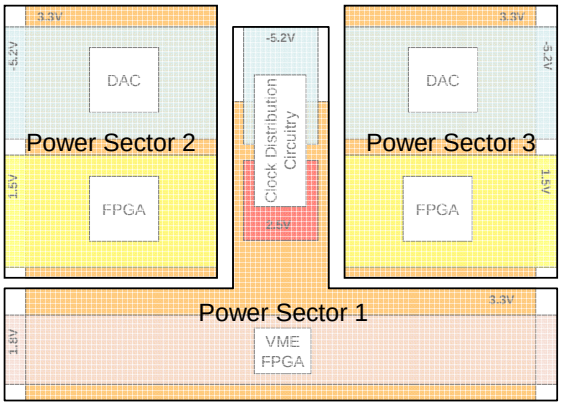


**Figure 3 - Power Distribution Diagram**

## 6. Power Measurement Circuit

This AWG includes a power measurement circuit for a self test to verify that the output level of the waveform generators are at the expected levels. The AWG can perform this test during the self test mode. In this mode the generated output is directed to the power measurement circuit through the switch. The VME bus FPGA will record the output of the test in a dedicated register which can be read by the host computer via the VME bus.

# IV. PERFORMANCE CHARACTERIZATION

These performance characterization results were gathered from tests of the single AWG prototype board that was made for the purpose of verifying the design concepts of this waveform generator. These tests were conducted

with a 720 MHz system clock because that is the clock rate being used for our application.

### 1. Amplitude Flatness

One of the primary advantages of an AWG is that there is opportunity for pre-distortion of the desired waveform in order to achieve the desired output characteristics. Amplitude flatness is one of the qualities that can be improved based on pre-distortion. Due to the fact that most of the amplitude variations in a DAC output results from the $\sin(x)/x$ roll-off, this amplitude variation can be corrected by scaling the waveform samples accordingly.

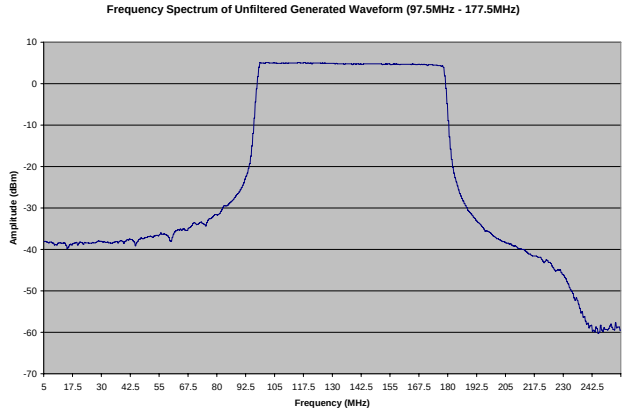


**Figure 4 - Chirp Output in Frequency Spectrum**

Figure 4 shows the output from the AWG without pre-distortion and only with low pass filtering at a cutoff of over 200MHz. The amplitude roll-off of less than 1dB across the passband can be corrected easily by scaling the samples prior to loading.

### 2. Phase Characterization

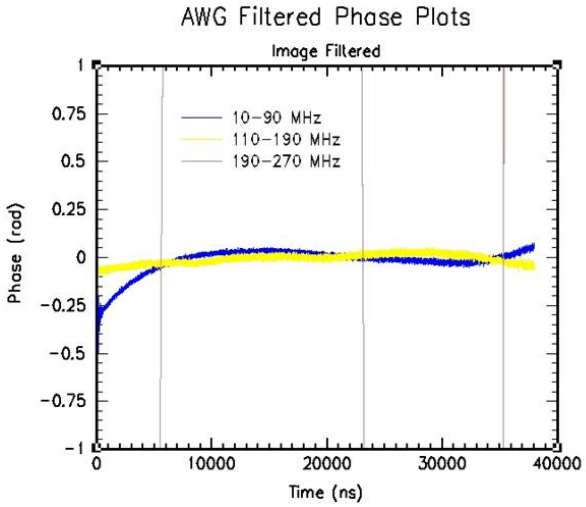


**Figure 5 - Phase Deviation from Quadratic Fit**

The AWG is able to achieve high phase fidelity in its generated waveform. Figure 5 shows the phase deviation of the output waveform as captured by a digital oscilloscope. In the figure we are comparing the phase unwrapped output, sampled by the oscilloscope, with the best quadratic fit. The results from figure 5 show a 1.2º RMS phase deviation on the AWG output.

### 3. Jitter Characterization

For radar applications, pulse to pulse jitter translates into random phase error that decreases resolution in the radar return data. We used a test devised for characterization of other chirp generators to determine the pulse to pulse timing jitter of this AWG. The test involved generating a waveform with frequency steps centered at a frequency $f_0$ and mixing this signal with a constant frequency waveform generated from a local oscillator (LO) of frequency $f_0$. Figure 6 shows the setup for this jitter test.

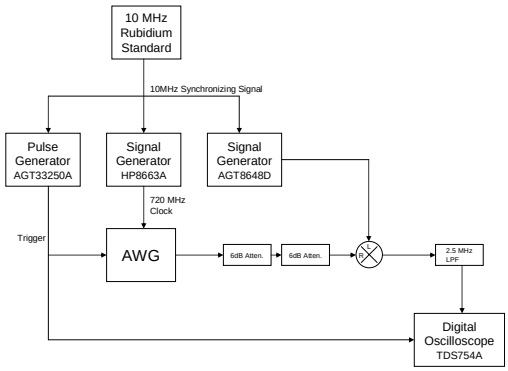


**Figure 6 - Jitter Test Setup**

The output will have a DC portion at the center where the generate waveform should match exactly in frequency with the input LO. Variations in this DC component can be converted to timing jitter via the formula:

$$\sigma_j = \frac{\sigma_a / 4}{2\pi f_0 A_0} \qquad (1)$$

$\sigma_a$ is the amplitude variation, $f_0$ is the center frequency of the generated waveform from the AWG, $A_0$ is the amplitude of the output of the test setup.

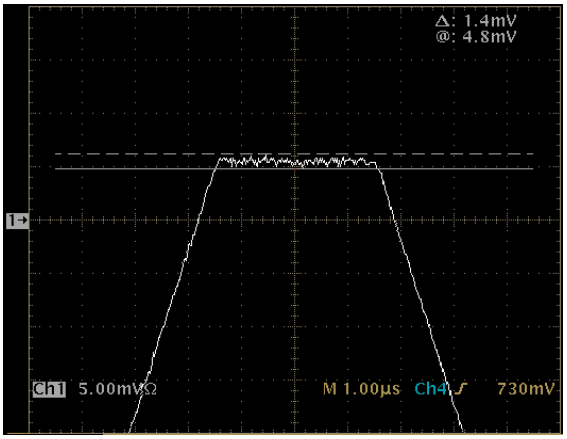


**Figure 7 - DC Variation in Single Jitter Test Output**

Figure 7 shows a single output of this jitter test. This variation is representative of the sample to sample timing jitter of the AWG.

Figure 8 shows the DC variation of the test output accumulated over thousands of pulses. In this graph the variation in the DC voltage level of the output is predominantly as a result of pulse to pulse jitter on the AWG output. In this case 4874 output pulses were captured to reveal that the pulse to pulse timing jitter resulting from the AWG is less than 12ps.

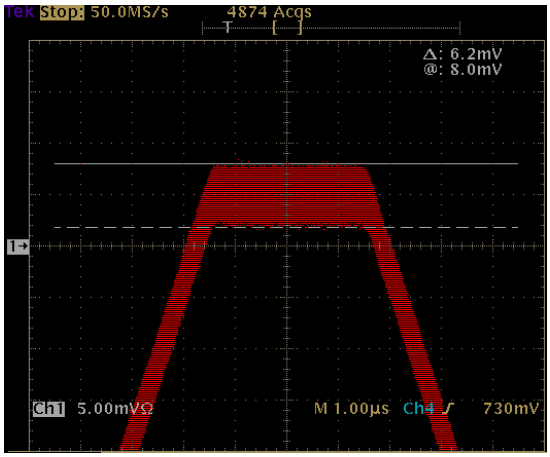


**Figure 8 - DC Variation in 4874 Jitter Test Output Waveforms**

## V. CONCLUSIONS

This AWG provides significant advantage in waveform flexibility, capability to generate two waveforms synchronously, as well as lower mass and power consumption compared to other AWGs. The basic architecture also allows for easy upgrade paths for improvements in achievable bandwidth and pulse length. The performance data of the AWG shows that it will be capable of providing waveforms to radar systems that will be able to operate with the highest precision, enabling radars to perform in many wide ranging applications.

## ACKNOWLEDGEMENTS

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## REFERENCES

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